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Automated Test Generation and Execution for Simulink

Traditional Software Testing is Costly

Software is an inherent part of many products, and its ever-growing complexity is increasing the cost of product development. Although many tools support software system design and implementation, few support verification, validation, and testing which accounts for 40% to 70% of development effort. Software verification and testing in many organizations is a manual process. It is inefficient and relies on testers' experience and judgment to find problems hidden throughout the system.

A Comprehensive Approach

T-VEC's Test Generation System for Simulink (Simulink Tester) provides an integrated solution for continuous model analysis, automatic test generation, test execution and results analysis. It analyzes every path throughout the model hierarchy and generates test vectors that exercise the path boundaries. Unreachable paths which result in dead code are identified and hyperlinked to the Simulink model elements involved. This test selection process produces unit, integration and systems test vectors most effective in revealing both decision and computational errors in logical, integer and floating-point domains.

Significant Benefits

T-VEC customers report savings between 40% and 60% of their development budgets while reducing test schedule by up to 90%. T-VEC solutions help product development teams integrate modeling with model analysis, and automated testing to eliminate labor-intensive, manual processes that cannot find bugs in complex systems.

Test design is the most labor-intensive and time-consuming testing activity consuming 60% of test effort.

Simulink Tester Features:

- Systematic, comprehensive test generation from Simulink models
- Unit, integration and system level tests
- Test sequences for testing dynamic systems
- Model defect identification
- Test drivers for any platform
- Simulation data for model validation
- Measurement and status reports for tracking project status
- Unrivaled test coverage:
  - Path Coverage
  - Decision Coverage
  - Condition Coverage (MC/DC)
  - Complete Hierarchy Coverage
  - Input Range Stressing
  - Boundary Value Stressing

The Benefits:

- Considerable competitive advantages from reduced schedule and costs
- Increased quality and reliability
- Enhanced test coverage
- Early defect identification
- Reduced risk to budgets and schedules
- Measurable project status, defects, and test coverage
- Testable models
- Reduced evolution and maintenance costs

Mature and Trusted

T-VEC has developed and refined the tools underlying the Simulink Tester for more than a decade to meet the needs of complex, mission-critical aircraft software systems. These tools have been used in software certifications with authorities such as the FAA and FDA. Although the roots of the technology were developed to meet the needs of ultra high assurance systems, T-VEC tools improve software quality in any industry's products whether embedded systems, information systems, or otherwise.

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We cover all boundaries of your software™

Model Analysis and Test Automation

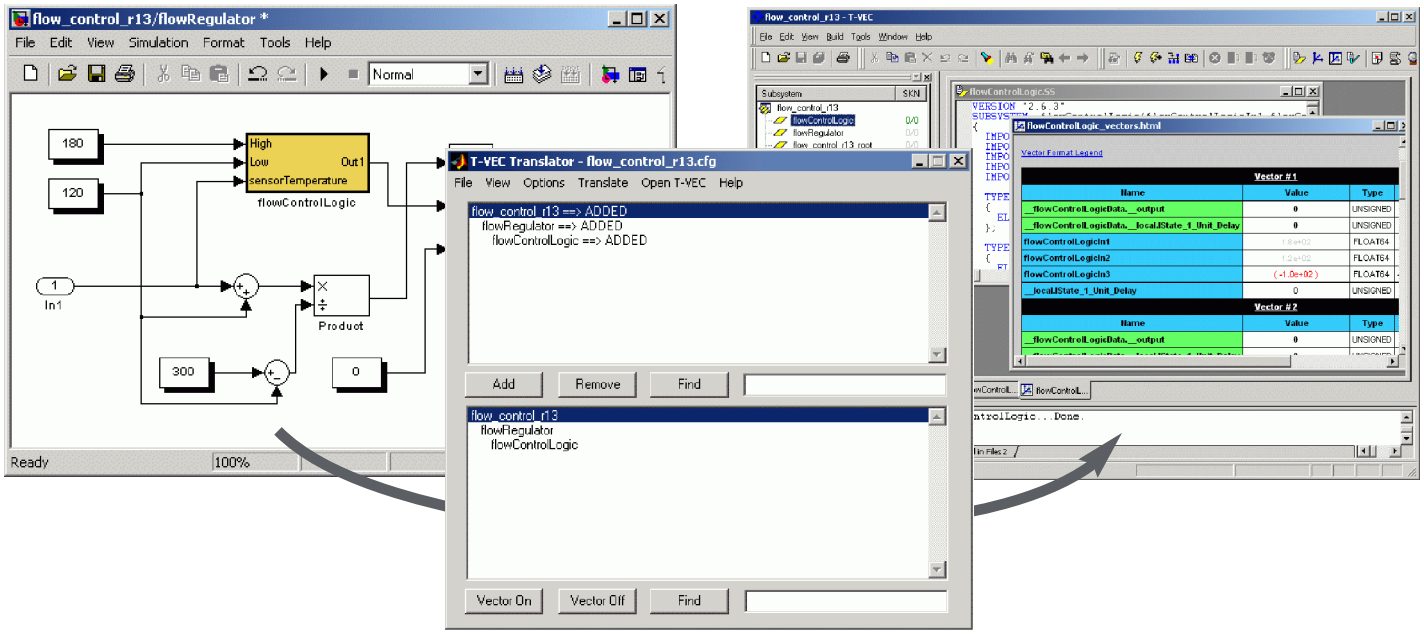
Project engineers use Simulink to model the software system and typically validate the model through simulation. Source code is then generated automatically from the model or developed manually. To test implementations of the model or generate simulation data, the engineer uses the Simulink Tester Graphical User Interface from within MATLAB to:

- Configure options for test generation
- Add signal range information
- Optionally configure test sequence generation
- Translate Simulink model to T-VEC

Within the T-VEC Test Vector Generation System, the engineer then:

- Analyzes model for defects
- Generates test vectors
- Generates test drivers
- Executes tests against code or within Simulink
- Generates test results report

The Simulink Tester creates T-VEC test specifications from Simulink models, then analyzes the test specifications to generate an optimal set of test vectors. During this process T-VEC identifies model errors, such as contradictions or inconsistencies, which can result in unachievable conditions or other undesirable properties. Test sequence vectors support verifying dynamic aspects of the system. Test driver generation transforms the test vectors from a generic format into test harnesses compatible with the code generated by the Real-time Workshop GRT and ERT code generators. These test harnesses are compiled in the same environment as the source code to generate a test program. This test program is executed in conjunction with the source code in the target environment. When the test driver executes, the results of each test are stored for comparison with the expected results. Finally, T-VEC tools compare actual test outputs to expected outputs to verify that the code implementation satisfies the model.



Model Capture
Model Simulation
Code Generation

Subsystem Selection
Translation Options
Signal Range Data

Model Analysis
Test Generation
Coverage Analysis
Test Driver Generation

Minimum System Requirements

- MATLAB R13, Simulink, RTW
- IBM PC or 100% compatible
- 1 GHz processor and 256MB RAM
- Microsoft Windows NT 4.0 SP3, 2000, XP

T-VEC Technologies, Inc.
2214 Rock Hill Road
Herndon, Virginia 20170-4227
www.t-vec.com
703.742.7100